WHAT IS CLAIMED IS:

1. An integrated circuit having a simultaneous bi-directional (SBD) input/output circuit, the SBD input/output circuit comprising:

a driver to drive an SBD transmission line in response to a driver input signal;

a receiver to compare a first voltage on the SBD transmission line to first and second reference voltages, and to output to the integrated circuit an input signal that depends upon the result of the comparison; and

reference selection circuitry to control at least one of the first and second reference voltages used by the receiver in response to the driver input signal.

2. The integrated circuit of claim 1, wherein the receiver comprises first and second differential amplifiers connected to a common output node, each differential amplifier having first and second input nodes, the first input node of each differential amplifier connected to the transmission line, the second input node of the first differential amplifier connected to the first reference voltage, the second input node of the second differential amplifier connected to the second reference voltage.

3. The integrated circuit of claim 2, wherein the common output node comprises first and second differential output nodes, the receiver further comprising first and second matched load resistors, the first load resistor connected between a first supply voltage and the first differential output node, the second load resistor connected between the first supply voltage and the second differential output node, and wherein each differential amplifier comprises:

a current source to generate a tail current at a tail node;

a first field-effect transistor having a gate connected to the first input node, a drain connected to the first differential output node, and a source connected to the tail current node;

and

a second field-effect transistor, matched to the first field-effect transistor, the second field-effect transistor having a gate connected to the second input node, a drain connected to the second differential output node, and a source connected to the tail current node.

4. The integrated circuit of claim 3, wherein the first and second differential amplifier current sources are matched to each other.

5. The integrated circuit of claim 4, wherein the first and second field-effect transistors of the first and second differential amplifiers are matched to each other.

6. The integrated circuit of claim 1, wherein the reference selection circuitry comprises a reference generator to generate the second reference voltage, the reference generator setting the second reference voltage to a high voltage when the driver input signal is a logic high voltage and setting the second reference voltage to a low voltage when the driver input signal is a logic low voltage.

7. The integrated circuit of claim 6, the reference generator comprising:

first and second complementary pass transistors having gates coupled to a common input node that receives the driver input signal, the first pass transistor passing a low voltage to an output node when activated, the second pass transistor passing a high voltage to the output node when activated.

8. The integrated circuit of claim 7, the first pass transistor having a drain connected to the second reference voltage that approximates the low voltage, the second pass transistor having

a drain connected to the second reference voltage that approximates the high voltage minus the threshold voltage of the second pass transistor.

9. The integrated circuit of claim 6, the reference generator comprising:

first and second transmission gates having a common output node and coupled to a common input node that receives the driver input signal such that when the driver input signal is a logic low voltage the first transmission gate is activated and when the driver input signal is a logic high voltage the second transmission gate is activated, the first transmission gate having an input connected to a low reference voltage, the second transmission gate having an input connected to a high reference voltage.

10. The integrated circuit of claim 6, wherein the reference selection circuitry further comprises a mid-voltage generator to generate the first reference voltage as a voltage midway between a high voltage and a low voltage.

11. The integrated circuit of claim 10, wherein the mid-voltage generator also generates the first reference voltage for other SBD circuits on the same integrated circuit.

12. The integrated circuit of claim 10, wherein the mid-voltage generator also exports the first reference voltage to a second integrated circuit connected to the transmission line.

13. The integrated circuit of claim 6, wherein the reference supply circuitry comprises a circuit input pad to receive the first reference voltage from an external reference.

14. The integrated circuit of claim 1, wherein the transmission line is integrated on the integrated circuit, and wherein the SBD input/output circuit communicates with another SBD input/output circuit on the same integrated circuit across the transmission line.

15. The integrated circuit of claim 1, wherein the driver comprises a resistor connected between a first supply voltage and an SBD transmission line terminal, a first transistor having a drain connected to the SBD transmission line terminal and a source connected to the drain of a second transistor, the second transistor having a source connected to a second supply voltage, wherein the gate of the first transistor receives a voltage signal approximately midway between the first and second supply voltages, and wherein the gate of the second transistor is controlled by the driver input signal.

16. An integrated circuit having a simultaneous bi-directional (SBD) input/output circuit, the SBD input/output circuit comprising:

a driver to drive an SBD transmission line in response to a driver input signal;

a receiver to compare a first voltage on the SBD transmission line to at least one of first and second reference voltages, and to output to the integrated circuit an input signal that depends upon the result of the comparison;

midpoint voltage generation circuitry that, when connected with similar circuitry on a second integrated circuit, generates a first midpoint voltage that approximates the voltage on the SBD transmission line when the driver is driving a logic high signal and a driver on the second integrated circuit is driving a logic low signal on the SBD transmission line, and generates a second midpoint voltage that approximates the voltage on the SBD transmission line when the driver is driving a logic low signal and the driver on the second integrated circuit is driving a logic high signal on the SBD transmission line; and

reference selection circuitry that selects the first midpoint voltage as the first reference voltage when the driver input signal is set to cause the driver to drive a logic high signal, and selects the second midpoint voltage as the first reference voltage when the driver input signal is set to cause the driver to drive a logic low signal.

17. The integrated circuit of claim 16, wherein the midpoint voltage generation circuitry comprises a first drive circuit having an output terminal where the first midpoint voltage exists and a second drive circuit having an output terminal where the second midpoint voltage exists, the first and second drive circuits matched respectively to the driver when driving a logic high signal and logic low signal.

18. The integrated circuit of claim 16, wherein the receiver receives the first midpoint voltage as an input to one transistor of a first differential transistor pair and receives the second midpoint voltage as an input to one transistor of a second differential transistor pair, and wherein the reference selection circuitry selectively activates one of the differential transistor pairs and deactivates the other differential transistor pair to select which of the midpoint voltages will be compared to the first voltage on the SBD transmission line.

19. A method of decoding remotely signaled data from the voltage of a simultaneous bi-directional (SBD) transmission line, the method comprising:

supplying a first reference voltage to a receiver, the first reference voltage having a predetermined voltage between a first voltage and a second voltage;

supplying a second reference voltage to the receiver, the second reference voltage selected from the first voltage and the second voltage in response to an input signal;

supplying the voltage on the SBD transmission line to the receiver, the intended voltage on the SBD transmission line selected from among the first voltage, the second voltage, and a midpoint voltage between the first and the second voltage;

comparing the voltage on the SBD transmission line to the first and second reference voltages; and

outputting, based on the comparison, a data signal representing the logic state of the remotely signaled data.

20. The method of claim 19, wherein comparing the voltage on the SBD transmission line to the first and second reference voltages comprises:

supplying the first reference voltage and the voltage on the SBD transmission line as inputs to a first differential transistor pair sharing a first tail current;

supplying the second reference voltage and the voltage on the SBD transmission line as inputs to a second differential transistor pair sharing a second tail current; and

driving a common load pair from both the first and second differential transistor pairs, such that a differential voltage taken across the load pair represents the result of both comparisons.

21. The method of claim 19, wherein supplying the second reference voltage comprises setting the second reference voltage to a high voltage when the locally signaled data is logic high and setting the second reference voltage to a low voltage when the locally signaled data is logic low.

22. The method of claim 19, wherein supplying the first reference voltage comprises supplying a voltage midway between a logic high voltage and a logic low voltage.

23. The method of claim 22, wherein supplying a voltage midway between a logic high voltage and a logic low voltage comprises:

generating a first midpoint voltage representative of the voltage on the SBD transmission line that would be expected when the remotely signaled data has a low logic state and the locally signaled data has a high logic state;

generating a second midpoint voltage representative of the voltage on the SBD transmission line that would be expected when the remotely signaled data has a high logic state and the locally signaled data has a low logic state; and

supplying the first midpoint voltage as the voltage midway between when the logic state of the locally signaled data is high, and supplying the second midpoint voltage as the voltage midway between when the logic state of the locally signaled data is low.

24. A simultaneous bi-directional (SBD) input/output circuit comprising:

a driver to drive a driver input signal to a transmission line;

a receiver that simultaneously compares a voltage on the transmission line to two different voltages and indicates which of the two different voltages is closer to the voltage on the transmission line; and

reference selection circuitry to set at least one of the two different voltages based on the state of the driver input signal.

25. A system comprising:

a first transmission line;

first and second integrated circuits, having respective simultaneous bi-directional (SBD) input/output circuits coupled through respective input/output pads to the first transmission line, wherein each SBD input/output circuit comprises a driver to drive a driver input signal, a receiver that simultaneously compares the voltage on the first transmission line to two different voltages and indicates which of the two different voltages is closer to the voltage on the first transmission line , and reference selection circuitry to set at least one of the two different voltages based on the state of the driver input signal.

26. The system of claim 25, further comprising reference generator circuitry on each of the first and second integrated circuits, the reference generator circuitry on the two circuits connected by at least a second transmission line to generate at least one of the two different voltages.